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EXAMINER	
FLORES, LEON	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/731,730	SONI ET AL.	
	Examiner	Art Unit	
	LEON FLORES	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims (1-20) have been considered but are moot in view of the new ground(s) of rejection.

Response to Remarks

Applicant asserts that *"an adjustment of the rate of a delay line does not suggest in any way a reduction in the length of the line, nor different input and output rates, as claimed in previous and currently amended claim 1. Warren does not disclose nor otherwise suggest reducing the length of the delay line, nor a delay line with an input rate smaller than an output rate. As previously discussed, the difference in rates results in a gap in data within the delay line that can be used to drop delay elements to reduce the length of the delay chain".*

The examiner agrees. However, a new ground of rejection has been issued.

Applicant further asserts that *"Applicant has previously argued that Alexander is from a non-analogous art and therefore cannot be relied upon as a basis for ejection of the claimed invention. The Examiner has replied in the Office Action of February 28, 2008, indicating that Alexander can be relied upon since both applicant's and Alexander's disclosure deal with synchronization. Applicant respectfully disagrees with this argument, as applicant's claimed invention deals not with synchronization, like Alexander, but with optimizing data path latency. In Alexander, an analog delay chain is adjusted for achieving synchronization between two clocks. In Applicant's claimed*

invention, a clocked delay chain is reduced for reducing data path latency. The particular problem with which the Applicant is concerned is not achieving synchronization, as in Alexander; therefore, Oetoker, 977 F. 2d 1443 24 USPQ2d 1443 (Fed. Cir. 1992), previously cited by the Examiner, does not apply".

The examiner respectfully disagrees. In response to applicant's argument that the reference of Alexander is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, the reference of Alexander does teach synchronization using a delay line, a multiplexer, and a controller. Furthermore, the rate and length of the delay line is adjusted using the multiplexer and the controller.

Applicant finally asserts that *"in Alexander, adjustment of the delay chain occurs while synchronization is incomplete, and the adjustment is directed at achieving synchronization. In Alexander, the delay chain is not adjusted in response to a signal of completion of a transient processing operation on the data samples, as recited in amended claim 1".*

The examiner agrees. However, a new ground of rejection has been issued.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. **Claims (1-8, 14) are rejected under 35 U.S.C. 103(a) as being unpatentable over Warren et al (hereinafter Warren) (US Patent 6,075,807) in view of Tweed et al. (hereinafter Tweed) (US Patent 5,818,769)**

Re claim 1, Warren discloses a method of reducing data path latency in digitally processing a sequence of data samples, the data path latency being associated with a transient processing operation on the data samples, comprising: during the transient processing operation on the data samples reading the sequence of data samples into a tapped clocked delay chain (See fig. 1 & col. 3, lines 40-54); during the transient processing operation on the data samples, processing data samples from taps on the clocked delay chain (See fig. 1 & col. 3, lines 40-54); and in response to receiving a signal of completion of a the transient processing operation on the data samples,

shifting data samples rapidly out of the clocked delay chain. (See fig. 1 & col. 4, lines 24-36)

But the reference of Warren fails to explicitly teach that it shifts data samples out of the delay chain at a higher output rate than an input rate of data samples coming into the clocked delay chain; and dynamically reducing the length of the clocked delay chain as data samples continue to be read into the clocked delay chain.

However, Tweed does. (See figs. 2A, 5) Tweed discloses that it shifts data samples out of the delay chain at a higher output rate than an input rate of data samples coming into the clocked delay chain (See col. 6, line 66—col. 7, line 5, col. 7, line 65 – col. 8, line 2); and dynamically reducing the length of the clocked delay chain as data samples continue to be read into the clocked delay chain. (See col. 8, lines 14-19)

Therefore, taking the combined teachings of Warren & Tweed as a whole, it would have been obvious to one of ordinary skills in the art to incorporate these features into the system of Warren, in the manner as claimed and as taught by Tweed, for the benefit of changing the throughput delay without interrupting the series of digital data elements. (See col. 7, lines 3-5)

Re claim 2, the combination of Warren & Tweed further discloses that wherein the data samples are from a data packet. (In Warren, see col. 2, lines 3-7, col. 2, lines31-35 "CDMA")

Re claim 3, the combination of Warren & Tweed further discloses that wherein

the data packet conforms to a transmission system selected from the group of 802.11 a, 802.11 g and HIPERLAN/2 transmission systems. (One skilled in the art would know that data packets may be used in a variety of different standards.)

Re claim 4, the combination of Warren & Tweed further discloses that wherein the transient processing operation includes a synchronization of the data packet. (In Warren, see col. 4, lines 33-36)

Re claim 5, the combination of Warren & Tweed further discloses that wherein the clocked delay chain comprises a plurality of pipelined registers. (In Warren, see fig. 1 & col. 3, lines 42-44)

Re claim 6, the combination of Warren & Tweed further discloses that wherein the reducing the length of the clocked delay chain is performed until a desired length of the clocked delay chain is achieved. (In Tweed, see col. 7, line 65 – col. 8, line 19)

Re claim 7, the combination of Warren & Tweed further discloses that wherein reducing the length of the clocked delay chain further includes bypassing empty registers. (In Tweed, see col. 7, line 65 – col. 8, line 19. Furthermore, it inherent and well known in the art to bypass registers in order to reduce the length of the delay line. This is mainly done in order to reduce power consumptions. See US 6,765,419)

Re claim 8, Warren discloses a method of reducing data path latency in digitally processing a sequence of data samples of a data packet, the data path latency being associated with synchronization of the data packet, comprising: upon reception of the data packet, reading the sequence of data samples from the a data packet into a tapped clocked delay chain comprising a plurality of pipelined registers (See fig. 1 & col. 3, lines 40-54); processing data samples from taps on the clocked delay chain to synchronize the a data packet (See fig. 1 & col. 3, lines 40-54); in response to receiving a signal of completion of synchronization of the data packet, shifting samples rapidly out of the clocked delay chain. (See fig. 1 & col. 4, lines 24-36)

But the reference of Warren fails to explicitly teach that it shifts data samples out of the delay chain at a higher output rate than an input rate of data samples coming into the clocked delay chain; reducing the length of the clocked delay chain by bypassing empty registers as data samples continue to be read into the clocked delay chain; and repeating the steps of shifting data samples rapidly out of the clocked delay chain at a higher output rate than the input rate and reducing the length of the clocked delay chain.

However, Tweed does. (See figs. 2A, 5) Tweed discloses that it shifts data samples out of the delay chain at a higher output rate than an input rate of data samples coming into the clocked delay chain (See col. 6, line 66—col. 7, line 5, col. 7, line 65 – col. 8, line 2); reducing the length of the clocked delay chain (See col. 8, lines 14-19) by bypassing empty registers as data samples continue to be read into the clocked delay chain (It is well known in the art to bypass empty registers in order to change the length of the delay line, see US 6,765,419); and repeating the steps of shifting data samples

rapidly out of the clocked delay chain at a higher output rate than the input rate and reducing the length of the clocked delay chain. (See col. 7, line 65 – col. 8, line 20)

Therefore, taking the combined teachings of Warren & Tweed as a whole, it would have been obvious to one of ordinary skills in the art to incorporate these features into the system of Warren, in the manner as claimed and as taught by Tweed, for the benefit of changing the throughput delay without interrupting the series of digital data elements. (See col. 7, lines 3-5)

Re claim 14, Warren discloses an apparatus comprising: means for reading data samples into a tapped clocked delay chain (See fig. 1 & col. 3, lines 42-54); means for processing data samples from taps on the clocked delay chain. (See fig. 1 & col. 3, lines 42-54)

Although the reference of Warren does teach adjusting the rate of the delay line after synchronization, it fails to explicitly teach means for shifting data samples out of the clocked delay chain at a higher output rate than an input rate of data samples coming into the clocked delay chain; and means for dynamically reducing the length of the clocked delay chain in response to receiving a signal of completion of a transient processing operation on the data samples.

However, Tweed does. (See figs. 2A, 5) Tweed discloses means for shifting data samples out of the clocked delay chain at a higher output rate than an input rate of data samples coming into the clocked delay chain (See col. 6, line 66—col. 7, line 5, col. 7, line 65 – col. 8, line 2); and means for dynamically reducing the length of the

clocked delay chain in response to receiving a signal of completion of a transient processing operation on the data samples. (See col. 8, lines 14-19)

Therefore, taking the combined teachings of Warren & Tweed as a whole, it would have been obvious to one of ordinary skills in the art to incorporate these features into the system of Warren, in the manner as claimed and as taught by Tweed, for the benefit of changing the throughput delay without interrupting the series of digital data elements. (See col. 7, lines 3-5)

5. **Claims (9-13, 19-20) are rejected under 35 U.S.C. 103(a) as being unpatentable over Warren et al (hereinafter Warren) (US Patent 6,075,807) in view of Alexander. (US Patent 6,765,419 B2)**

Re claim 9, Warren discloses an apparatus comprising: a pipeline of registers that store data samples (See fig. 1 & col. 3, lines 42-44); logic circuitry which controls each individual register of the pipeline of registers (See col. 4, lines 34-36); and a processor which controls the data shifting rates, the logic circuitry. (See fig. 1 & col. 4, lines 24-36)

But the reference of Warren fails to teach a multiplexer having inputs from select registers from the pipeline of registers, and an output; and the output of the multiplexer based on completion states of a transient processing operation on the data samples.

However, Alexander does. (See fig. 3 & col. 6, lines 23-54) Alexander discloses a multiplexer (99) having inputs from select registers from the pipeline of registers, and an output (76); and the output of the multiplexer based on completion states of a

transient processing operation on the data samples. (See fig. 2: 52, 56, 58 & col. 6, lines 4-22 "based on the phase difference of COMP signal controller 58 will either increase, decrease or leave unchanged the amount of time by which delay circuit 52 delays the output. Furthermore, one skilled in the art would have founded obvious to use this type of delay line (designer's choice) in Warren in order to adjust the rate of the delay line.

Therefore, taking the combined teachings of Warren & Alexander as a whole, it would have been obvious to one of ordinary skills in the art to incorporate these features into the system of Warren, in the manner as claimed and as taught by Alexander, for the benefit of changing the length of the delay line. (See col. 6, lines 16-19)

Re claim 10, the combination of Warren & Alexander further discloses that wherein the data samples are from a data packet. (In Warren, see col. 2, lines 3-7, col. 2, lines31-35 "CDMA")

Re claim 11, the combination of Warren & Alexander further discloses that data packet conforms to 802.1 la, 802.11 g and HIPERLAN/2 transmission systems standards. (One skilled in the art would know that data packets may be used in a variety of different standards.)

Re claim 12, the combination of Warren & Alexander further discloses a timing recovery module for synchronization of the data packet that initiates a transition in the processor. (In Warren, see col. 4, lines 33-36)

Re claim 13, Warren discloses an apparatus comprising: a pipeline of registers that stores data samples of a data packet (See fig. 1 & col. 3, lines 42-44); a timing recovery module for synchronization of the data packet that initiates a transition (See fig. 1 & col. 4, lines 24-40); logic circuitry which controls each individual register of the pipeline of registers. (See fig. 1 & col. 4, lines 24-40)

But the reference of Warren fails to explicitly teach a processor having inputs from a timing recovery module for packet synchronization which controls the data shifting rates, the logic circuitry.

However, the reference of Warren does suggest a processor having inputs from a timing recovery module for packet synchronization which controls the data shifting rates, the logic circuitry. (See fig. 1: 18 & col. 4, lines 24-40)

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Warren, in the manner as claimed, for the benefit of achieving synchronization.

The reference of Warren discloses the limitations as claimed above, except he fails to teach a multiplexer having inputs from select registers from the pipeline of registers, and an output; and the output of the multiplexer based on a plurality completion states of the synchronization of the data packet processing events of the apparatus.

However, Alexander does. (See fig. 3 & col. 6, lines 23-54) Alexander discloses a multiplexer (99)having inputs from select registers from the pipeline of registers, and an output (76); and the output of the multiplexer based on a plurality completion states

of the synchronization of the data packet processing events of the apparatus. (See fig. 2: 52, 56, 58 & col. 6, lines 4-22 "based on the phase difference of COMP signal controller 58 will either increase, decrease or leave unchanged the amount of time by which delay circuit 52 delays the output. Furthermore, one skilled in the art would have founded obvious to use this type of delay line (designer's choice) in Warren in order to adjust the rate of the delay line.

Therefore, taking the combined teachings of Warren & Alexander as a whole, it would have been obvious to one of ordinary skills in the art to incorporate these features into the system of Warren, in the manner as claimed and as taught by Alexander, for the benefit of changing the length of the delay line. (See col. 6, lines 16-19)

Re claim 19, the combination of Warren & Alexander fails to explicitly teach that wherein the processor is a state-machine.

However, the reference of Alexander does teach a control circuit capable of controlling the length of the delay line by using a multiplexer. The functionality of the control circuit is the same as of the state machine in applicant's claimed invention.

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Warren, as modified by Alexander, in the manner as claimed, for the benefit of changing the length of the delay line. (See col. 6, lines 16-19)

Claim 20 has been analyzed and rejected w/r to claim 19 above.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. **Claims (15-17) are rejected under 35 U.S.C. 102(b) as being anticipated by Tweed et al. (hereinafter Tweed) (US Patent 5,818,769)**

Re claim 15, Tweed discloses within a digital processor, a method of reducing data path latency in digitally processing data samples comprising: providing a clocked delay chain with an output rate higher than an input rate (See figs. 2A, 5 & col. 6, line 66—col. 7, line 5, col. 7, line 65 – col. 8, line 2); shifting data samples out of the clocked delay chain at the higher output rate while reading additional data samples into the input end of the clocked delay chain at the input rate in response to receiving a signal of completion of a transient processing operation on the data samples (See col. 6, line 66—col. 7, line 5, col. 7, line 65 – col. 8, line 2); and dynamically reducing the length of the delay chain as data samples continue to be read into the clocked delay chain. (See col. 8, lines 14-19)

Re claim 16, Tweed further discloses bypassing an empty portion of clocked delay chain. (See col. 8, lines 14-19. Furthermore, it inherent and well known in the art to bypass registers in order to reduce the length of the delay line. This is mainly done in order to reduce power consumptions. See US 6,765,419)

Re claim 17, Tweed further discloses performed in response to receiving a signal of completion of a processing event. (See col. 6, line 66 – col. 7, line 5, col. 7, line 65 - col. 8, line 19)

8. **Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tweed et al. (hereinafter Tweed) (US Patent 5,818,769) in view of Warren et al (hereinafter Warren) (US Patent 6,075,807)**

Re claim 18, Tweed further discloses that wherein the data samples are from a data packet. (See col. 4, lines 31-41)

But the reference of Tweed fails to explicitly teach that the signal of completion of a processing event is a sync signal indicating synchronization of the data packet.

However, Warren does. (See fig. 1 & col. 4, lines 24-36) Warren discloses that the signal of completion of a processing event is a sync signal indicating synchronization of the data packet.

Therefore, taking the combined teachings of Tweed & Warren as a whole, it would have been obvious to one of ordinary skills in the art to incorporate these features into the system of Tweed, in the manner as claimed and as taught by Warren, for the benefit of adjusting the propagation rate of the delay line.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LEON FLORES whose telephone number is (571)270-1201. The examiner can normally be reached on Mon-Fri 7-5pm Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/L. F./
Examiner, Art Unit 2611
June 1, 2009
/Shuwang Liu/
Supervisory Patent Examiner, Art Unit 2611